Claims

1. An electronic package assembly, comprising:

a plurality of semiconductor devices, each having a first side with a plurality of conductive pads, at least two of the plurality of devices being vertical power transistor devices having a second side opposite the first side, the second side having further conductive pads;

a printed circuit substrate, having a plurality of printed circuit patterns bonded to the conductive pads of the first sides of the plurality of semiconductor devices, and arranged to provide logic interconnections between the plurality of semiconductor devices; and,

a leadframe including leads which provide external connections for the package assembly, and having a non-lead island portion bonded to the further conductive pads of the second sides of the at least two vertical power transistor devices,

wherein the island portion of the leadframe forms a power interconnection between the at least two vertical power transistor devices.

2. The assembly of claim 1 wherein the leadframe further comprises a substrate lead portion, which is arranged to connect to a further pad of the printed circuit substrate, thereby directly connecting the leadframe to the substrate.

3. The assembly of claim 2 wherein the substrate lead portion is connected to the island portion of the leadframe such that the conductive pads of the second sides of the semiconductor devices are directly electrically connected to the substrate.

4. The assembly of claim 1 wherein a discrete electronic device is mounted directly onto the leadframe.

5. The assembly of claim 4 wherein the leadframe has contact bumps to which the electronic device is coupled.

6. The assembly of any preceding claim wherein the at least two semiconductor devices form a vertical H-bridge power transistor arrangement.

7. The assembly of any preceding claim the at least two semiconductor devices form a full-bridge high-sided switch arrangement.

8. The assembly of any preceding claim wherein the substrate has a first face having the plurality of pads, and a second face opposite the first face to which further electronic devices are attached.

9. The assembly of claim 8 wherein the substrate is provided with electrical vias arranged to electrically interconnect the first and the second faces of the substrate.

10. The assembly of any preceding claim wherein the substrate is provided with thermal vias arranged to sink heat away from the semiconductor device.